14. Flip Chip Technologies

Course Leader: Shengmin Wen – TATA

Course Objectives:
Advanced packaging, such as CSP, FCBGA, 2.5D/3D, HBM packaging, heterogenous with multiple-dies and multiple-Si-node packaging, embedded die packaging, certain wafer level package or panel level packaging, is based on flip chip technologies. For high-speed, high-performance application such as AI targeted design, flip chip technology is a must. Even some traditional packaging types such as QFN begin to use flip chip technology. Industry wise in terms of total annual revenue Flip chip packaging has grown steadily and already passed wire bond-based packaging.

This course will cover the fundamentals of flip chip assembly technologies, including major assembly processes, wafer bumping technologies, substrate types and critical BOM selection, design rules, and reliability modeling/evaluation.

Two major assembly processed, their related equipment, materials, design rules, and design practices are covered in detail. Examples are presented to demonstrate the versatile flip-chip integrations, including single die, monolithic multi-die, multi-level multi-die, as well as multi-form mixed interconnection that uses both wire bond / flip chip integration.

In-depth discussions include chip package interaction (CPI), package warpage control, substrate technologies, failure modes and root cause analysis, reliability tests, the important roles of electrical and mechanical simulation in the designs of a robust package, Si die floor plan optimization, design rules, among others. Students will understand the many options of flip chip technologies and learn a range of criteria that they can apply to their future projects.

Various bumping technologies that are used in today's flip chip assembly are also briefly introduced, i.e., lead-free solder bumping and highly customized Cu-Pillar bumping. The course will also cover various failure modes related to bumping, such as barrier consumption, Kirkendall void formation, non-wets, BEOL dielectric cracking, electromigration, etc.

A group exercise at the end of the class is planned to serve as an in-class capstone project, making sure that the students can walk away with an in-depth understanding of the flip chip assembly technologies, and are ready to apply the knowledge to their real-world packaging designs and projects.

Course Outline:
1. Introduction to Flip-Chip Technologies
2. Flip Chip Technologies: Mass Reflow Process
3. Flip Chip Technologies: Thermal Compression
4. Flip Chip Substrate Technologies
5. Underfill, Package Warpage Control, and Yield Detractors
6. Failure Modes, Examples, Modeling and Reliability Life Assessment
7. Flip Chip Si Package Co-Design on Various Types (BOT, BOP, AI Type) and Examples
8. Variations: Wafer Level CSP, Waver Lever Fan-Out, Panel Level Packaging, Hybrid Bonding
9. Bumping Process, Rules, and Introduction
10.Flip Chip Under-Bump Metallization and Intermetallic
11.Review and Package Selection Exercise – Group Discussions

Who Should Attend:

Anyone who wants to understand the fundamentals of flip chip packaging technology are encouraged to take this highly condensed and yet knowledge content fully covered course. These include graduate students who look for a packaging engineering career, engineers who are to take advanced package projects, project managers who want to have an in-depth technical understanding every step of the way, and managers who want to expand their understanding of key aspects of flip chip technologies to flawlessly adopt to company's product roadmap. This course may help materials and equipment vendors to understand the applications.

Bio: Dr. Shengmin Wen has more than 25 years of semiconductor industry experience in the areas of Si fabrication technology, advanced packaging and assembly process development, Si and packaging co-design, semiconductor device failure analysis, reliability and qualification, product engineering, testing, and volume production business management. Recent years, he focuses on Si and package co-design that uses the most advanced flip chip integration methods, in particular organic RDL for 2.5D and 3D chiplet based integration, in addition to development of panel-based packaging that uses chip last flip chip methodologies. He has extensive and unique experiences in flip chip assembly technologies that use fine pitch Cu Pillar bump with both mass reflow and thermal compression processes. He is an expert in package warpage control, substrate technologies, advanced fine pitch flip chip assembly process, and reliability assessment. He currently works for TATA Electronics as Vice President, and he previously worked for JCET as VP and GM of design service BU, Synaptics Inc as the principal packaging architect, and Amkor Technology as director of 3D PoP and CSP Product Business Group.

Dr. Wen received his Ph.D. from Northwestern University, Evanston, IL, USA, researching on fatigue and reliability of electronic materials, where he created and published a science-based fatigue theory. Dr. Wen has been actively participating and contributing to industry technical conferences to learn, to share, and to contribute.